X86 GPIO Testing Guidance

1. Install the Intel GPIO Configuration software;

2017-08-01 15:44	文件夹	
2017-08-01 15:44	文件夹	
2016-03-15 5:23	配置设置	12 KB
2016-03-15 5:23	图标	51 KB
2016-03-15 5:23	应用程序	1 543 KB
	2017-08-01 15:44 2017-08-01 15:44 2017-08-01 15:44 2017-08-01 15:44 2016-03-15 5:23 2016-03-15 5:23	2017-08-01 15:44 文件夹 2017-08-01 15:44 文件夹 2017-08-01 15:44 文件夹 2017-08-01 15:44 文件夹 2016-03-15 5:23 配置设置 2016-03-15 5:23 图标

	Application	2017-08-01 15:43	文件夹	
	BinData	2017-08-01 15:43	文件夫	
	Drivers	2017-08-01 15:43	文件夹	
	GPIODocuments	2017-08-01 15:44	文件类	
	Share	2017-08-01 15:44	文件夫	
	UEFI	2017-08-01 15:44	文件夫	
	XMLTemplates	2017-08-01 15:44	文件夹	
63	IIF2.ini	2016-03-15 5:23	配置设置	
w	Intel.ico	2016-03-15 5:23	图标	
H	Setup.exe	2016-03-15 5:23	应用程序	



2. Test method

2.1 Double click Intel GPIO Configuratio;



2.2 Select "Dirdect(HW) "



2.3 Select "ULT" ----≻ OK

📴 Intel® GPIO Configuration Tool		- 0	×
File Options Report Help			_
Target:		Intel® GPIO Configuration Tool	(intel)
Access:		Version 2.0.11	(index
GPIO Configuration			
	Query Platform		
	Platform:SkyLake		
	Select Platform Type:		
	O ULX O ULT O DI O Halo		
	ОК		
Busy			

2.4 Choose the red table, eg YS--I56200U motherboard, see below where marked yellow

arget: S	kyLake ULT												Intel®	GPIO	Confi	guratie	on Tool	A.
ccess: D	irect															Versio	n 2.0.11	
10 Conf	iguration			_														_
ommuni	ty 0 Communi	ty 1 Con	nmunity 2	2 Cor	mmunity ?	8												
SPIO In	GPIO Name	PadRstC	RXPadS	IntS	PMode	RXTXEnCfg	Term	RXRAW	GPIOTx5	RxEvC	RXIN	GPIRoutIO	GPIRou	GPIOR	GPIOT)	CFG0 \	CFG1 \	Open
SPP_A_C	CLKOUT_LPC_I	Dee ~	Raw ~		Nat ~	PadMode Cor	20k *	NoC ~	Leve ~	Di ~	N ~	NoPeri ~	Nc ~	Dit ~	Die 🕤	0x4400	0x0000	Upda
SPP_A_1	CLKOUT_LPC_	Dee *	Raw ~		Nat ~	PadMode Cor	20k *	NoC *	Levi ~	Di *	N *	NoPeri *	Nc *	Dit *	Dis *	0x4400	0x0000	Upda
SPP_A_1	PMEB	Dee *	Rav ~		GPII Y	PadMode Cor	Nor *	NoC Y	Levi *	Le *	N *	Periph *	Nc *	En *	Dit "	0x4010	0x000x0	Upda
SPP_A_1	BM_BUSYB_ISI	Pow *	Raw ~		GPI ~	PadMode Cor	Nor *	No(*	Levi ~	Di	N *	NoPeri *	Nc *	Die *	En "	0x0400	0x0000	Upda
GPP_A_1	SUSWARNB_S	Dee *	Raw ~	-	Nat ~	PadMode Cor	Nor *	No(*	Levr ~	Di *	N *	NoPeri *	Nc *	Dit *	Die *	0x4400	0x0000	Upda
SPP_A_1	SUS_STATB_ES	Dee 👻	Raw ~		Nat 🜱	PadMode Cor	Nor *	NoC *	Levi ~	Di *	N *	NoPeri Y	Nc *	Dit *	Dis "	0x4400	0x0000	Upda
SPP_A_1	SUSACKB	Dee *	Raw ~		Nat 🖌	PadMode Cor	20k *	No(*	Leve ~	Di *	N *	NoPeri *	Nc *	Dit ~	Die "	0x4400	0x0000	Upda
SPP_A_1	SD_1P8_SEL	Dee ~	Raw Y		Nat ~	PadMode Cor	Nor *	No(*	Levi ~	Di Y	N *	NoPeri *	Nc *	En. *	Dit *	0x4400	0x0000	Upda
SPP_A_1	SD_PWR_EN_E	Dee ~	Raw ~		Nat ~	PadMode Cor	Nor *	No(*	Leve "	Di *	N °	NoPeri ~	Nc *	Dit *	Dit "	0x4400	0x0000	Upda
GPP_A_1	ISH_GP_0	Dee *	Raw ~		GPI ~	PadMode Cor	Nor *	No(*	Leve ~	Le *	N *	NoPeri *	Nc *	Dit *	En "	0x4000	0x0000	Upda
GPP_A_1	ISH_GP_1	Dee ~	Raw ~	-	GPII ~	PadMode Cor	Nor *	No(+	Levr ~	Di *	N ~	NoPeri *	Nc ×	Dit *	En v	0x4400	0x0000	Upda
GPP_A_2	ISH_GP_2	Dee *	Raw ~		GPI ~	PadMode Cor	Nor *	NoC +	Leve ~	Di Y	N *	NoPeri *	Nc ×	Die *	En v	0x4400	0x0000	Upda
GPP_A_2	ISH_GP_3	Dee v	Raw ~	-	GPI ~	PadMode Cor	Nor *	NoC v	Levr ~	Le v	N ~	NoPeri *	Nc *	Dit ~	En v	0x4000	0x0000	Upda
GPP_A_2	ISH_GP_4	Dee *	Raw ~	1	GPI ~	PadMode Cor	Nor *	No(*	Levi *	Di *	N *	NoPeri *	Nc ×	Die *	En "	0x4400	0x0000	Upda
GPP_A_2	ISH_GP_5	Dee 👻	Raw ~	1	GPII ~	PadMode Cor 💚	Nor *	NoC v	Levi ~	Le v	N *	Periph *	Nc *	Dit v	En "	0x4010	0x0000	Upda
GPP_B_0	CORE_VID_0	Dee Y	Raw Y	1	Nat 🗵	PadMode Cor	Nor	NoC Y	Leve Y	Di Y	N Y	NoPeri Y	Nc.Y	Dis Y	Dis Y	0x4400	0x0000	Upda
GPP_B_0	CORE_VID_1	Dee ~	Raw ~	14	Nat ~	PadMode Cor	Nor *	NoC ~	Levi ~	Di *	N ~	NoPeri v	Nc ×	Dit v	Die 🗸	0x4400	0x0000	Upda
GPP_B_0	VRALERTB	Dee *	Raw ~		Nat ~	PadMode Cor 👻	Nor *	No(*	Levi Y	Di *	N *	NoPeri *	Nc Y	Di: *	Die *	0x4400	0x0000	Upda
GPP_B_0	CPU_GP_2	GPIL ~	Raw ~		GPII ~	PadMode Cor	Nor *	NoC ~	Levi ~	Le ~	N ~	Periph ~	Nc ~	En. ~	Dit "	0x8010	0x0000	Upda
GPP_B_0	CPU_GP_3	Dee ~	Raw ~	-	GPI 4	PadMode Cor	Nor *	No(*	Leve ~	Di *	N ~	NoPeri ~	Nc ~	Dit *	En "	0x4400	0x0000	Upda
GPP_B_0	SRCCLKREQB_	Dee ~	Ran ~		GPI ~	PadMode Cor	Nor ·	Not ~	Levr ~	Le ~	N v	Periph ~	Nc ~	En ~	Die "	0x4010	0x0000	Upda

2.5 Eg GP3 on rang where I marked with "1",--->"2" select enable --->"3" update to enable GP3;

arget: SkyLake	ULT												Intel®	GPIO	Confi	guratio	n Tool	(int
ccess: Direct																Versio	n 2.0.11	0
PIO Configuratio	n					-												
ommunity 0 C	ommuni	ty 1 Con	nmunity 2	Cor	mmunity :	3	19-2	1					1152002211			1		1.2
GPIO In GPIO	Name	PadRstC	RXPadS:	IntS	PMode	RXTXEnCfg	Term	RXRAW	GPIOTx5	RxEvC	RXIN	GPIRoutIO	GPIRou	GPIOR	GP OT	CFG0 \	CFG1 \	Opera
SPP_A_C SERIRO	2	Dee ~	Raw ~	1	Nat ~	PadMode Cor	Nor ~	No("	Leve ~	Di "	N ~	NoPeri *	Nc ~	Di: "	Dit *	0x4400	0x0000	Updat
SPP_A_C PIRQA	В	Dee Y	Raw ~		GPII Y	PadMode Cor	Nor *	No(*	Levi *	D) *	N Y	NoPeri *	Nc *	Dis "	En. Y	0x4400	0x0000	Updat
SPP_A_C CLKRU	NB	Dee Y	Raw ~		Nat ~	PadMode Cor	Nor *	No(*	Levr *	Di M	NY	NoPeri *	Nc *	Dis *	Dis Y	0x4400	0x0000	Updati
SPP_A_C CLKOL	IT_LPC_I	Dee Y	Raw ~		Nat ~	PadMode Cor	20k *	No(*	Levi ~	Di "	N Y	NoPeri *	Nc *	Dis *	Dis *	0x4400	0x0000	Updati
SPP_A_1 CLKOL	T_LPC_	Dee Y	Raw ~	1	Nat 🜱	PadMode Cor	20k *	No(*	Levi *	Di "	N *	NoPeri *	Nc *	Di: *	Dis Y	0x4400	0x0000	Updat
SPP_A_1 PMEB		Dee *	Raw ~		GPII ~	PadMode Cor	Nor *	No(*	Levi *	Le "	N *	Periph *	Nc *	En *	Dis *	0x4010	0x0000	Updat
SPP_A_1 BM_BU	ISYB_ISI	Pow Y	Raw ~	1.0	GPI Y	PadMode Cor	Nor *	No(*	Leve *	Di "	N *	NoPeri *	Nc *	Dit *	En. ~	0x0400	0x0000	Updat
SPP_A_1 SUSW	ARNB_S	Dee ~	Raw ~		Nat ~	PadMode Cor	Nor *	No(*	Levi *	Di Y	N *	NoPeri *	Nc "	Di: "	Dit "	0x4400	0x0000	Updat
SPP_A_1 SUS_S	TAT8_ES	Dee Y	Raw ~	$[[\mathcal{T}]]$	Nat ~	PadMode Cor	Nor *	No(*	Levi *	Di *	N.Y	NoPeri *	Nc *	Die Y	Dis *	0x4400	0x0000	Updat
SPP_A_1 SUSAC	KB	Dee *	Raw ~		Nat 👻	PadMode Cor	20k *	No(v	Levi *	Di "	N ~	NoPeri *	Nc *	Di: *	Dir *	0x4400	0x0000	Updat
SPP_A_1 SD_1P	B_SEL	Dee Y	Raw ~	1.	Nat 🜱	PadMode Cor	Nor Y	No(v	Lev: Y	Di "	N Y	NoPeri Y	Nc Y	En Y	Dis Y	0x4400	0x0000	Updat
GPP_A_1 SD_PW	R_EN_E	Dee ~	Raw ~	-	Nat ~	PadMode Cor	Nor v	No(v	Levi ~	Di "	N ~	NoPeri Y	Nc v	Dit "	Dit *	0x4400	0x0000	Updat
SPP_A_1 ISH_G	0_0	Dee *	Raw ~		GPII -	PadMode Cor	Nor *	No(v	Levi ~	Le "	N ~	NoPeri *	Nc Y	Dit *	En. v	0x4000	0x0000	Updat
SPP_A_1 ISH_G	21	Dee ~	Raw ~		GPII ~	PadMode Cor	Nor ~	No(v	Levi ~	Di v	N ~	NoPeri ~	Nc ~	Dit "	En. ~	0x4400	0x0000	Updat
GPP_A_2 ISH_GI	2_2	Dee Y	Rav ~		GPI ~	PadMode Cor	Nor *	No(*	Levi ~	Di Y	N *	NoPeri Y	Nc Y	Di: *	En. Y	0x4400	0x0000	Ilpdat
GPP_A_2 ISH_GI	2.3	Dee ~	Rav ~		GPI ~	PadMode Cor	Nor ~	No(v	Leve ~	Le "	N v	NoPeri Y	Nc ~	Die	En. 🛩	0x4000	0x000x0	Updet
GPP_A_2 ISH_GI	4	Dee v	Rav ~	1.4	GPI ~	PadMode Cor	Nor *	No(*	Levi Y	Di v	N *	NoPeri Y	Nc v	Dis	Enable	0x4400	0x000x0	Updat
GPP_A_2 ISH_GI	25	Dee v	Ravs ~		GPI +	PadMode Cor	Nor ~	No(v	Leve ~	Le "	N ~	Periph v	Nc v	Die	Disable	0x4010	0x0000	Updat
SPP_B_0 CORE_	VID_0	Dee ~	Raw ~		Nat ~	PadMode Cor	Nor "	No(~	Leve ~	Di "	N ~	NoPeri *	Nc. "	Dis "	Dis ~	0x4400	0x0000	Updat
SPP_B_0 CORE_	VID_1	Dee ~	Raw ~	-	Nat ~	PadMode Cor	Nor "	NoC v	Levi ~	Di ~	N ~	NoPeri 👻	Nc *	Die "	Dis ~	0x4400	0x0000	Updat
SPP_B_C VRALE	RTB	Dee ~	Raw ~		Nat ~	PadMode Cor	Nor ~	NoC *	Leve ~	Di ~	N ~	NoPeri Y	Nc *	Dis "	Dis ~	0x4400	0x0000	Updat
	-	-			-		1		-		-			_	-		-	-

2.6 on "1" Pmode range, select GPIO Mode ---> update;

larget: S	kyLake ULT Direct												Intel®	GPIO	Confi	guratio Versio	n Tool n 2.0.11	ín
PIO Conf	iguration															2012		
ommuni	ty 0 Communi	ity 1 Cor	mmunity 2		mmunity	3				_			_		_		_	
GPIO In	GPIO Name	PadRstC	RXPadSt	IntS	PMade	RXTXEnCfg	Term	RXRAW	GPIOT	BxEvC	RXIN	GPIRoutiO	GPIRou	GPIOR	GPIOT	CEG0 \	CEG1 \	Onera
SPP_A_C	SERIRQ	Dee ~	Raw ~		Nat ~	PadMode Cor	Nor *	NoC ~	Leve ~	Di ~	N -	NoPeri Y	Nc ~	Dis "	Dis ~	0x4400	0x0000	Updat
SPP_A_C	PIRQAB	Dee *	Raw ~		GPH ~	PadMode Cor	Nor *	No(*	Leve ~	Di *	N *	NoPeri *	Nc *	Dit "	En. ~	0x4400	0x0000	Updat
SPP_A_C	CLKRUNB	Dee *	Raw ~	-	Nat ~	PadMode Cor	Nor *	No(*	Levi Y	Di Y	N *	NoPeri *	Nc *	Di: *	Dis *	0x4400	0x0000	Updat
SPP_A_C	CLKOUT_LPC_I	Dee *	Raw ~	-	Nat ~	PadMode Cor	20k *	No(*	Levr *	D: *	N *	NoPeri Y	Nc Y	Dis V	Dis *	0x4400	0x0000	Updat
PP_A_1	CLKOUT_LPC_	Dee *	Raw ~	4	Nat ~	PadMode Cor	20k *	No(*	Levi "	Di *	N *	NoPeri *	Nc *	Die v	Dis Y	0x4400	0x0000	Upda
SPP_A_1	PMEB	Dee Y	Raw ~	-	GPIK ~	PadMode Cor "	Nor *	No(*	Leve "	Le ~	N. *	Periph *	Nc *	En. "	Dit "	0x4010	0x0000	Upda
SPP_A_1	BM_BUSYB_ISI	Pow *	Raw ~	-	GPIK ~	PadMode Cor *	Nor *	No(*	Leve *	Di *	N ~	NoPeri *	Nc *	Dit *	En. Y	0x0400	0x0000	Upda
SPP_A_1	SUSWARNB_S	Dee Y	Raw ~	-	Nat ~	PadMode Cor	Nor *	NoC ~	Levi *	Di Y	N *	NoPeri *	Nc *	Dit *	Dis 👻	0x4400	0x0000	Upda
SPP_A_1	SUS_STATB_ES	Dee *	Raw ~	-	Nat ~	PadMode Cor	Nor *	No(*	Leve Y	Di *	N. *	NoPeri *	Nc *	Dit *	Dis *	0x4400	0x0000	Upda
SPP_A_1	SUSACKB	Dee *	Raw ~	-	Nat ~	PadMode Cor	20k *	No(v	Levi *	D: *	N *	NoPeri *	Nc v	Di: *	Dis *	0x4400	0x0000	Upda
SPP_A_1	SD_1P8_SEL	Dee *	Raw ~	-	Nat ~	PadMode Cor	Nor *	No(*	Levi Y	Di *	N *	NoPeri Y	Nc v	En. *	Dis *	0x4400	0x0000	Upda
GPP_A_1	SD_PWR_EN_E	Dee v	Raw ~	-	Nat ~	PadMode Cor	Nor *	No(v	Levi Y	Di Y	N *	NoPeri v	Nc ×	Dis v	Dis Y	0x4400	0x0000	Upda
GPP_A_1	ISH_GP_0	Dee v	Raw ~	4	GPIL Y	PadMode Cor	Nor *	No(*	Levi Y	Le *	N *	NoPeri Y	Nc *	Di: Y	En. Y	0x4000	0x0000	Upda
GPP_A_1	ISH_GP_1	Dee v	Raw ~	-	GPIK ~	PadMode Cor	Nor *	No(+	Levi Y	Di Y	N *	NoPeri Y	Nc *	Di: *	En. v	0x4400	0x0000	Upda
GPP_A_2	ISH_GP_2	Dee *	Raw ~	-	GPI ~	PadMode Cor	Nor *	No(*	Leve Y	Di *	N *	NoPeri 👻	Nc *	Dit "	En. Y	0x4400	0x0000	Upda
GPP_A_2	ISH_GP_3	Dee v	Raw Y	2	GPIK ¥	PadMode Cor	Nor *	No(+	Leve Y	Le ~	N *	NoPeri v	Nc v	Dit Y	En. Y	0x4000	0x000x0	UBia
GPP_A_2	ISH_GP_4	Dee *	Raw ~	GPI	O Mode	PadMode Cor	Nor *	No(~	Leve Y	Di Y	N *	NoPeri *	Nc *	Dit *	En. v	0x4400	0x0000	Upda
GPP_A_2	ISH_GP_5	Dee v	Raw Y	Nat	tive Fn1	PadMode Cor	Nor *	No(v	Levi Y	Le *	N *	Periph Y	Nc v	Dis 👻	En. v	0x4010	0x000x0	Upda
GPP_B_0	CORE_VID_0	Dee 👻	Raw ~	Nat	tive Fn2	PadMode Cor	Nor ~	No(~	Levi ~	Di ~	N ~	NoPeri ~	Nc *	Dit ~	Dis 👻	0x4400	0x0000	Upda
GPP_B_0	CORE_VID_1	Dee ~	Raw ~		Nat	PadMode Cor	Nor *	No(~	Levi ~	D: ~	N *	NoPeri *	Nc *	Di: "	Dis "	0x4400	0x0000	Updat
GPP_B_0	VRALERTB	Dee ~	Raw ~		Nat °	PadMode Cor	Nor ~	NoC ~	Levi ~	Di ~	N ~	NoPeri *	Nc ~	Dis ~	Dis 🔍	0x4400	0x0000	Upda

2.7 On "1"GPIOTxS range--->select level 0/level1 --->update for high and low level switching.

arget: SI	kyLake ULT												Intel®	GPIO	Confi	guratio	n Tool	(int
coess: D	irect															Versio	n 2.0.11	-
10 Confi	guration								_									
ommunit	y 0 Communi	ty 1 Con	nmunity 2	Cor	nmunity 3	8			1	1								
SPIO In	GPIO Name	PadRstC	RXPadS	IntS	PMode	RXTXEnCfg	Term	RXRAW	GPIOTx5	RxEvC	RXIN\	GPIRoutIO	GPIRou	GPIOR	GPIOT	CFG0 \	CFG1 \	Opera
PP_A_C	SERIRQ	Dee *	Rav. ~		Nat *	PadMode Cor	Nor *	No(*	Levi ~	Di ~	N *	NoPeri *	Nc *	Dit *	Dit ~	0x4400	0x0000	Updat
PP_A_C	PIRQAB	Dee *	Ran ~		GPII *	PadMode Cor	Nor *	No("	Levi *	Di Y	Nº Y	NoPeri *	Nc Y	Die *	En "	0x4400	0x0000	Updat
PP_A_C	CLKRUNB	Dee *	Raw ~		Nat Y	PadMode Cor 👻	Nor *	No(*	Leve Y	Di *	N *	NoPeri Y	Nc *	Dit *	Dit *	0x4400	0x0000	Updat
SPP_A_C	CLKOUT_LPC_I	Dee *	Rav ~		Nat *	PadMode Cor	20k *	No("	Leva Y	Di *	N Y	NoPeri 👻	Nc *	Dit *	Dit "	0x4400	0x0000	Updat
SPP_A_1	CLKOUT_LPC_	Dee *	Raw ~		Nat ~	PadMode Cor	20k *	No(*	Levi *	Di Y	N *	NoPeri *	Nc *	Dit *	Dit *	0x4400	0x0000	Updat
PP_A_1	PMEB	Dee *	Raw ~	Ψ.	GPII ~	PadMode Cor	Nor *	No(*	Levi *	Le "	N: *	Periph *	Nc ~	En *	Dis *	0x4010	0x0000	Updat
PP_A_1	BM_BUSYB_ISI	Pow *	Raw ~	×.	GPIC Y	PadMode Cor	Nor *	NoC Y	Levi Y	Di *	N *	NoPeri Y	Nc Y	Dit *	En Y	0x0400	0x0000	Updat
PP_A_1	SUSWARNB_S	Dee *	Raw ~		Nat ~	PadMode Cor	Nor *	No("	Levi *	Di *	N *	NoPeri *	Nc *	Die Y	Dis *	0x4400	0x0000	Updat
PP_A_1	SUS_STATB_ES	Dee *	Raw ~		Nat Y	PadMode Cor	Nor *	No(*	Levi *	Di *	Nº Y	NoPeri *	Nc Y	Dis *	Die *	0x4400	0x0000	Updat
PP_A_1	SUSACKB	Dee ~	Rav. ~	Ξ.	Nat ~	PadMode Cor	20k *	No(*	Levi Y	Di *	N . 4	NoPeri *	Nc *	Dit *	Die *	0x4400	0x0000	Updat
PP_A_1	SD_1P8_SEL	Dee Y	Raw ~	v	Nat Y	PadMode Cor	Nor Y	No(*	Lew Y	D: Y	N. *	NoPeri Y	Nc ×	En ×	Die 👻	0x4400	0x0000	Updat
PP_A_1	SD_PWR_EN_E	Dee ~	Raw ~	×.	Nat ~	PadMode Cor	Nor *	No(*	Levi Y	Di *	N Y	NoPeri *	Nc v	Dis ~	Die v	0x4400	0x0000	Updat
PP_A_1	ISH_GP_0	Dee v	Raw ~	v	GPII Y	PadMode Cor	Nor *	No(*	Levi ~	Le v	N *	NoPeri *	No Y	Dis ~	En v	0x4000	0x0000	Updat
PP_A_1	ISH_GP_1	Dee v	Raw ~	~	GPIr ~	PadMode Cor	Nor *	No(~	Levi ~	Di ~	N	NoPeri Y	Nc *	Dis ~	En v	0x4400	0x0000	Updat
PP_A_2	ISH_GP_2	Dee *	Raw ~	~	GPII Y	PadMode Cor	Nor *	No(·	Levi *	Di v	N *	NoPeri v	Nc v	Dir v	En v	0x4400	0x0000	Lipsiph
PP_A_2	ISH_GP_3	Dee ~	Rav. ~	1	GPII ~	PadMode Cor	Nor *	No(~	Levio	Le ~	N. ~	NoPeri ~	Nc ×	Dit *	En v	0x4000	0x0000	Uplat
PP_A_2	ISH_GP_4	Dee *	Raw ~	Y	GPII Y	PadMode Cor	Nor *	No(*	Level 0	Di Y	N: *	NoPeri v	Nc *	Di: *	En. v	0x4400	0x0000	Updat
PP_A_2	ISH_GP_5	Dee v	Rav. ~	- Q.	GPI v	PadMode Cor	Nor v	No(~	Level 1	Le ~	N. 4	Periph ~	Nc ~	Dit *	En v	0x4010	0x0000	Updat
PP_B_0	CORE_VID_0	Dee ~	Ran ~		Nat ~	PadMode Cor	Nor *	No(v	Leve ~	Di ~	N ~	NoPeri ~	Nc ~	Dir "	Die Y	0x4400	0x0000	Updat
PP_B_0	CORE_VID_1	Dee v	Raw ~	0	Nat ~	PadMode Cor	Nor *	No(*	Leve ~	Di v	N. v	NoPeri ~	Nc v	Dir *	Die v	0x4400	0x0000	Updat
PP_B_C	VRALERTB	Dee "	Ray ~	-	Nat ~	PadMode Cor	Nor *	No("	Leve ~	D ~	N "	NoPeri ~	Nc -	Die -	Die .	0x4400	0x0000	Undat
-				_	TTAT			1001		-			146	10712		Sec. or other		opaul